

Incorporating Synopsys CAD Tools In Teaching VLSI Design

Puteri Megat Hamari

Minnesota State University Mankato

Abstract

VLSI Design is a course for graduate and undergraduate students at the Minnesota State University, Mankato to introduce students to the theory, concepts and practice of VLSI design. For Spring 2015, the course syllabus was changed with the integration of industrial grade VLSI CAD using Synopsys. Previously, simulations were limited and performed with open source software. With Synopsys, students used methodology similar to the process used in industry to design complex circuits. This paper describes the experience of an instructor in teaching VLSI Design and how the instructor has successfully integrated the teaching of CMOS theory, process technology and complex logic design through the use of Synopsys tools. Topics covered in this paper include course outline, the use of CAD sessions to teach design skills, the ability of students to use basic circuit blocks to build larger designs and how the methodology of teaching evolved with the use of Synopsys.

Keywords

VLSI, Synopsys, CAD tool, design layout, hands-on learning

Introduction

The fast changing technological innovations in the Very Large Scale Integrated (VLSI) industry gives rise to new challenges in training new engineers for the industry. Exposure to industry grade EDA (*electronic design automation*) in undergraduate and graduate courses allow students to be systematically prepared to enter the industry and be prepared for any challenges.

VLSI Design has been offered as a course (EE584/484) at Minnesota State University, Mankato since 1990 to graduate and undergraduate students. However, the course was previously theory based with most instruction occurring in class. A supplementary and *optional* lab utilizing open source CAD (*computer-aided design*) and simulation software was initially offered but it was not popular with the students and was gradually phased out. None of the previous instructors tried to use mainstream commercial CAD tools such as those from Cadence or Synopsys to do the lab. This is a significant drawback as this methodology resulted in students who were mainly exposed to the theory of VLSI design but without any actual experience in doing hands-on design. The instructor believes that it is important to prepare and give the students the opportunity and experience of using tools that are currently used in industry.

This paper will discuss how the instructor made the use of the Synopsys EDA tools an integral part of a one-semester VLSI design course where the syllabus covers the spectrum of VLSI design beginning with MOS transistor theory and CMOS process technology, circuit and logic design through the synthesis and design of digital systems. This was the first time that industrial-grade IC design tools were used as the primary toolset.

This paper discusses the course content, hands-on exercises, final project design and the effectiveness of using a state-of-the-art, industry-grade CAD tool in the introduction and instruction of VLSI design to students.

Course Outline

The course material for EE584/484 covered everything from MOS transistor theory and CMOS process technology through circuit and logic design, to the design and creation of complex digital systems. The syllabus and focus of VLSI Design was changed for the Spring 2015 class to incorporate the use of an industrial grade VLSI CAD using Synopsys modern EDA tools. Synopsys Inc. includes the use of a generic 90nm library that mirrors a CMOS manufacturing process¹. This allowed the incorporation of CAD sessions into the syllabus with the primary goal of allowing the students to gain hands-on experience of designing VLSI circuits with tools that are industry grade.

In the newly redesigned course, students are exposed to the theoretical underpinnings of VLSI design in classes and the CAD sessions are used to fortify their understanding of the material. The use of the Synopsys EDA is only covered in the CAD sessions and the session material seeks to let the students test their knowledge in a practical manner. The course does not have a laboratory session attached to the lectures, however as the instructor believes in the importance of hands-on experience using the CAD tools, the instructor added “CAD sessions”, which are separate from the in-class instruction and is dedicated to learning and working on the CAD tool. In the beginning of the course, the students were in the classroom for 3 hours of lectures a week. Later, the students were in the classroom for 2 hours of lectures a week and were expected to spend 1 -1/2 hours per week outside the classroom time on the software tools.

The first CAD session, in the fourth week of the semester, was to introduce the students to the Synopsys tools. Figure 1 is the course outline that shows the incorporation of CAD sessions and the materials covered in the course in the semester. The early CAD sessions were individual exercises where students learnt to draw the layouts of basic CMOS gates and simulated them using the software tool. They learnt how to lay down design layouts within the constraints of minimum scaling rules. The in-class lectures prepared the students with the knowledge to calculate parasitic capacitances and resistances and predict the propagation delay of their designs. Their hands-on work allowed the use of simulation to verify their calculation and predictions. In their class project, they worked in teams of three students to design a fairly complex circuit that was built up from basic cells that they had designed in earlier CAD sessions.

**2015 ASEE Zone III Conference
(Gulf Southwest – Midwest – North Midwest Sections)**

WEEK	TOPIC
1	Course Introduction
	VLSI Physical Design
	Design Technique
2	MOS Transistor Theory – Device Physics
	MOS Transistor Theory – Structure
3	MOS Transistor Theory – IV Characteristics
	MOS Transistor Theory – Scaling
	MOS Transistor Theory – Capacitance
4	CAD Session – Introduction to Synopsys
	Modeling of MOS using SPICE – DC Analysis
	Modeling of MOS using SPICE – Transient Response
5	Exam 1
	MOS Fabrication Process & Physical Design
	MOS Inverters – Static Characteristics
6	Propagation delay estimation
	Power estimation, yield, and scaling
	CMOS logic design styles
7	MOS Inverters – Switching Characteristics
	CAD Session – Inverter Simulation
	Combinational Logics
8	Combinational Logics
	CAD Session – NAND Layout
	Sequential MOS Logic Circuits
9	Sequential MOS Logic Circuits, Schmidt Trigger
	Schmidt Trigger, Phase Locked Loop
	Latches, flip-flops, and registers
10	Clocking strategies, CMOS IC design options
	CAD Session – NAND Simulation
	Dynamic Logic Circuits
11	Dynamic Logic Circuits
	CAD Session
	Exam 2
12	Memory SRAM
	Memory DRAM
	CAD Session Project Assignment
13	Design and Implementation Methodology
	Design and Implementation Methodology
	Arithmetic Building Block
14	Arithmetic Building Block
	CAD Session – Work on project
	CAD Session – work on project
15	CAD Session – work on project
	CAD Session – work on project
	CAD Session – work on project
16	Final Project Due

Figure 1: Course outline: Sequence of materials covered in the semester and CAD sessions.

Students were introduced to the methodology of VLSI design by allowing them to first design simple standard cells that are then used as building blocks for more complex circuits. The culmination of the course is a team project that were chosen from several challenging designs for implementation.

During the last quarter of the semester, the systems perspective of VLSI design and implementation methodology was highlighted. Students learnt this through the

implementation of high-speed adders. The knowledge learnt from this was then put into practice for their team-based project design, which was the culmination of the course and will be discussed later in this paper. As this course is an introductory course, the subject of IC testing and design of tests were not covered. These are topics which can be better addressed by a higher-level course.

CAD Session Materials

The instructor was able to take full advantage of the extensive resources that Synopsys Inc. provides for University Program members². These includes information and material that the instructor can use for classroom and CAD sessions such as tutorials and guides on how to use the CAD tools.

The Synopsys interoperable Process Design Kits (PDKs) is used by MSU Mankato for this course. This is a PDK that is not constrained by intellectual property restrictions for academic and research purposes. This Synopsys PDK contains the following: technology files: physical verification files, parasitic extraction files, Spice models, schematic symbols, PCells, and scripts³.

In the initial CAD session, students went through a tutorial that demonstrates how to use and run the Synopsys Custom Designer (CDesigner) tool on a Linux workstation. The CDesigner tool allows students to assemble a schematic circuit and create a layout. Figure 2 shows the example of students' work. Hspice and WaveView are used together with the CDesigner to simulate and view the output waveforms. Students learned to create a testbench for the circuit schematic to test the circuit. The testbench provides the stimulus to the circuit and students performed the DC and transient analysis in the simulation and analysis environment (SAE) as shown in Figure 3.

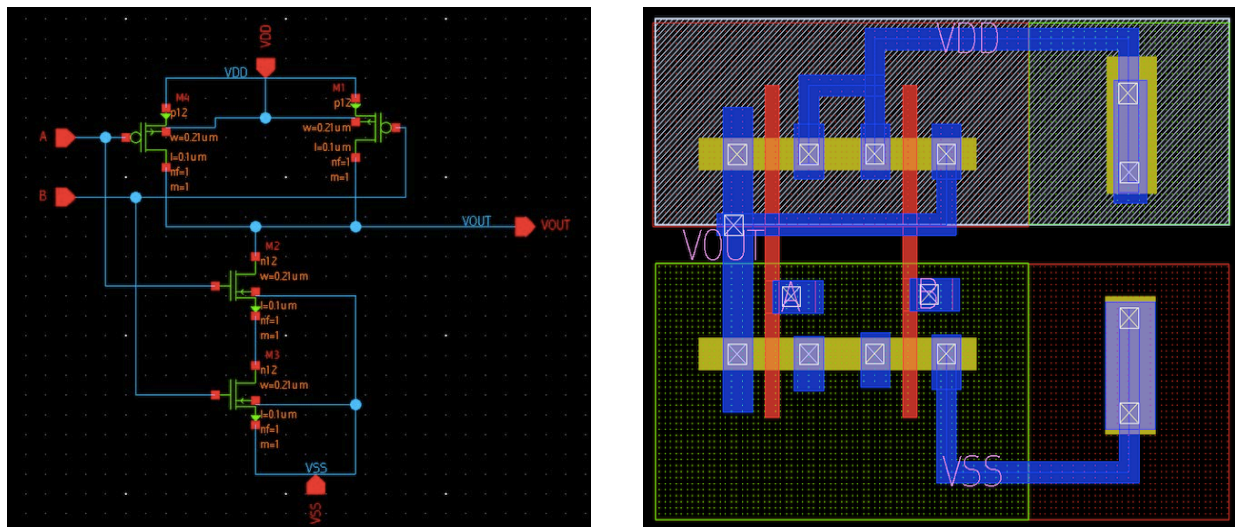


Figure 2: Example of students' work using schematic and layout editor. (Left) Schematic layout of NAND gate at the transistor level. (Right) Physical layout of the NAND gate drawn using the Custom Designer layout editor.

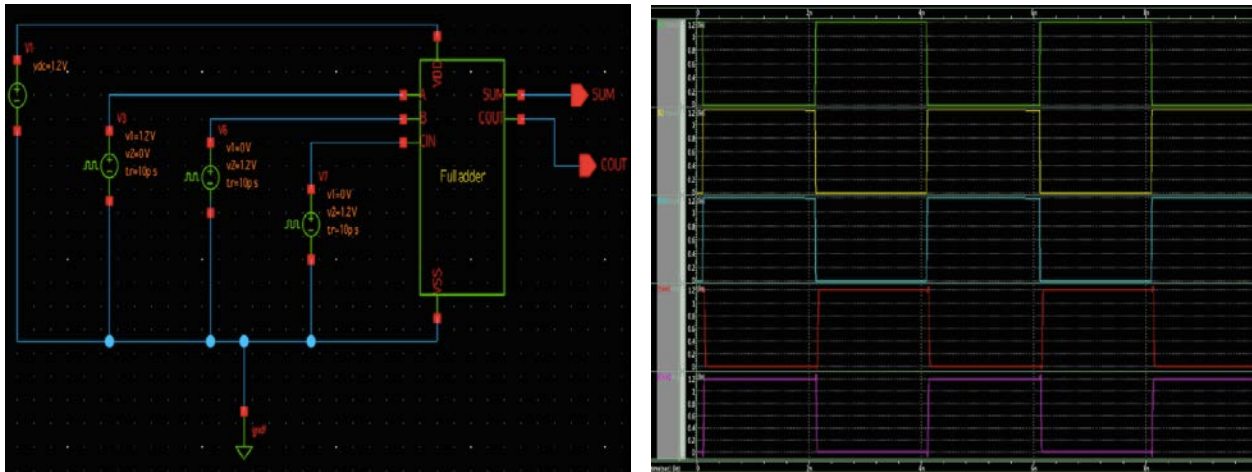


Figure 3: (Left) Example of a testbench for a 1-bit full adder taken from a team’s project. (Right) Simulation output waveform with SAE using WaveView.

Students followed a Synopsys tutorial that includes detailed step-by-step instructions on how to do schematic entry, layout entry, verification, and pre-layout and post layout simulations². The first task was for the students to create an inverter. This was a simple task to get the students to be familiar with the tools and the process of designing. The end purpose was to achieve mastery of the process and transferring that skill into the design of a more complex circuit. While the next CAD session was not until the next few weeks, the students were expected to spend 1-1/2 hour a week outside the classroom to use the software. This was necessary as it was their first time using the software. As with any complex software, there was a steep learning curve in learning the steps to create and simulate the inverter. However the students were excited to do the task as they realized the importance of learning an integrated set of industry-grade design tools in their academic career. This was a skill that was directly transferable to industry if they were to seek a profession in this field. Figure 4 shows the Synopsys custom design flow and the tools used in each stage.

Once the students were finished with the simulation of the inverter, they would then draw the inverter layout using the Layout Editor. The layout of the inverter that they drew must match the transistors’ size in the schematic stage. To run a design rule check (DRC) on the layout based on the technology process, a tool called IC validator was used. The same tool was used to make sure the inverter layout matched the schematic by running a Layout Versus Schematic (LVS) check.

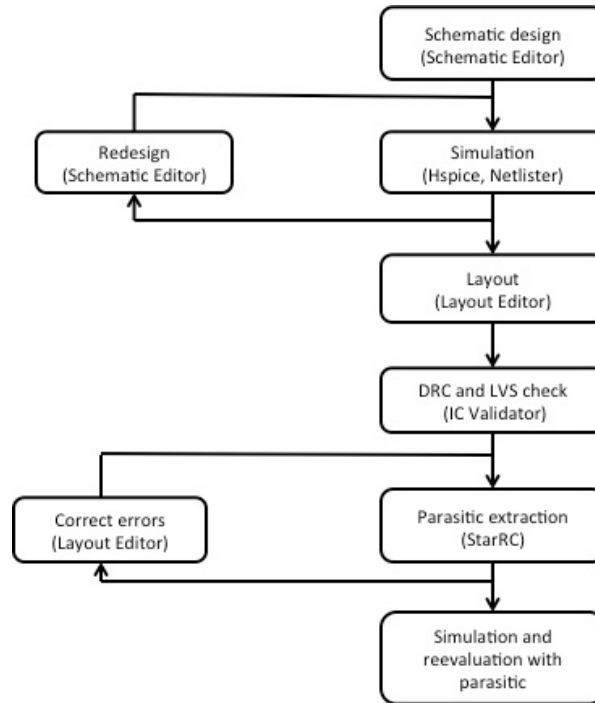


Figure 4: Custom design flow chart¹.

After the students had completed the inverter layout without errors, they were asked to design two- and three- input NAND gates. This followed the same process as the inverter. The second time around was simpler for the students as they had mastered the process and were familiar with the tools. These basic gates would be used in their team design project.

Course Design Project

The culmination of the VLSI course was a team project on a full custom design of a fairly complex circuit using 90nm CMOS technology through the Synopsys EDA. The two criteria for the design were: 1) the design had to be hierarchical and make use of the basic cells that they had designed in their CAD sessions and 2) the complexity of the project must be manageable for a team of 3 students for completion in 4 weeks. Several project ideas that were provided for the students were:

- 4-bit carry-lookahead adder/subtractor
- 4-bit A to D converter
- 4-bit multiplier
- 4-bit random number generator
- vending machine

Students were also given a choice to choose or create their own unique design that was sufficiently complex to perform any task or application. They were free to submit their own proposals as long as it met the two criteria outlined earlier. In their designs, students had to take into account parasitic capacitances, propagation delay and layout area. The goal was to minimize all three. The success of their design was gauged through an optimization metric

based on the product of these three parameters. The project design and report were due on the final exam week. All groups successfully completed the physical layout and simulation. Figure 5 shows the example of a 4-bit full adder layout from a team's work. However, none of the groups had time to successfully simulate the extraction of the parasitic parameters for their design. As an alternative, they were asked to do hand calculations to estimate the parasitic parameters of their design as part of the component in their design report.

The instructor required all the students to provide their unbiased opinion on their experience in doing the design project using the Synopsys EDA tools. The majority had a positive experience and enjoyed learning how to use the Synopsys EDA. They all stated that they learned a lot from the work performed for the CAD sessions and the group project. They also wished that they had more time to perform the assigned work.

The instructor plans changes to the course based on the students' experience. The course will be changed to a 4 credit hour course from the current 3 credit hour course and there will be dedicated lab sessions that will be compulsory. This will provide more time for the students to work on the assigned work as well as their team project. In the longer time frame, the instructor plans to move the course to the Fall semester. This will allow for the students' projects to be submitted to MOSIS for fabrication and they will be able to receive the fabricated circuits to be tested. This would make designing for tests an integral part of the students final project.

Summary

This paper shows how the instructor successfully implemented the use of an industry-grade design tool into the syllabus of an introductory VLSI design course. Separating the theoretical instruction from the CAD sessions allowed the course to cover the entire spectrum of VLSI design starting with MOS transistor theory through gate and logic design and culminating with a team project that utilized the design and synthesis of complex digital systems. The Synopsys EDA proved to be a great tool for introducing students that are new to VLSI design, the nuances and complexities of the process of designing and synthesizing complex circuits.

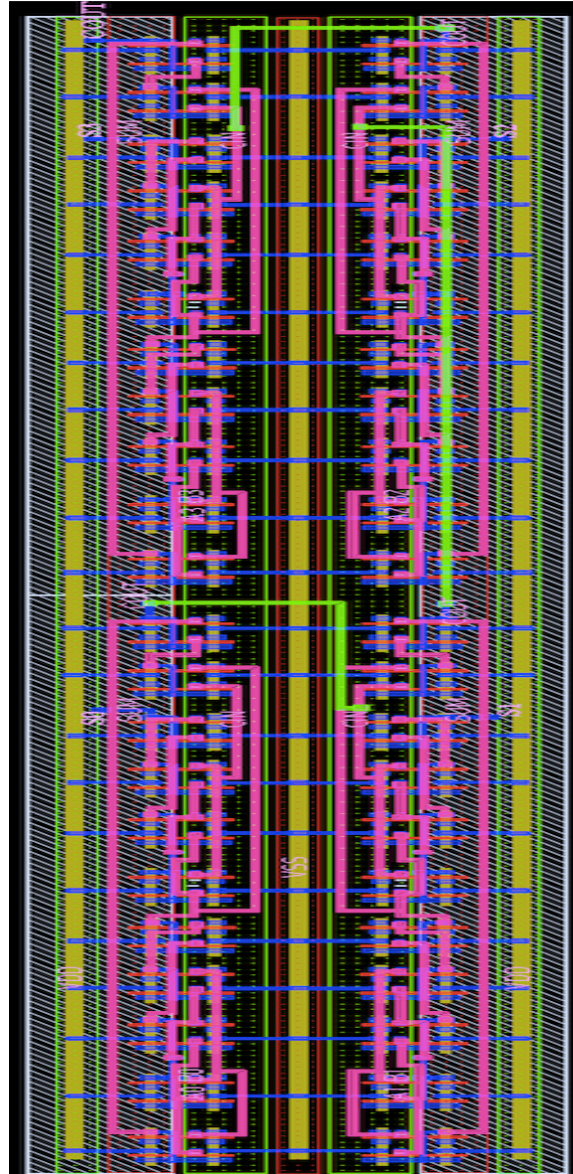


Figure 5: Example layout of a 4-bit full adder from a team's project.

Students were excited to learn to use the tools as they feel that they were mastering a skill that is directly transferable to industry. Learning how to use industry grade EDA tools gives them a feel for how the industry does complex projects. Students believe that the exposure to the design and synthesis of a complex circuit through the Synopsys EDA provides them with an experience that will allow them to stand out among their peers when they seek employment in the VLSI field.

References

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Puteri Megat Hamari

Since 2012, Puteri Megat Hamari has served as an Assistant Professor at Minnesota State University Mankato, she is currently in the Department of Electrical and Computer Engineering and Technology, where she teaches courses in digital logic, circuit analysis, integrated circuit fabrication and VLSI design. Previously, she was with the Integrated Engineering Department where she was involved in project-based learning for engineering. Dr. Megat Hamari received a B.Sc., M.S., and Ph.D. in Electrical Engineering from Vanderbilt University in Nashville, Tennessee. Dr. Megat Hamari is actively involved in research in fabricating micro fuel cells and joint research in photonics.